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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/811,430	03/26/2004	Sehat Sutardja	MP0185.D2	2961
23624	7590	03/16/2005	EXAMINER	
MARVELL SEMICONDUCTOR, INC. INTELLECTUAL PROPERTY DEPARTMENT 700 FIRST AVENUE, MS# 509 SUNNYVALE, CA 94089			NGUYEN, MATTHEW VAN	
			ART UNIT	PAPER NUMBER
			2838	

DATE MAILED: 03/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/811,430

Applicant(s)

SUTARDJA ET AL.

Examiner

MATTHEW V. NGUYEN

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 26 March 2004.  
2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-87 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 1-87 is/are rejected.  
7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.  
10) ☒ The drawing(s) filed on 26 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 3/30/04 and 6/1/04.  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.  
5) ☐ Notice of Informal Patent Application (PTO-152)  
6) ☐ Other: \_\_\_\_\_.

1. The disclosure should be carefully reviewed and ensure that any and all grammatical, idiomatic, and spelling or other minor errors are corrected.
2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 4, 6-10, 13-15, 18, 20-24, 27-29, 32, 34-38, 41-43, 49-53, 56-58, 64-68, 71-73, 79-83, 86 and 87 are rejected under 35 U.S.C. 102(b) as being anticipated by Sluijs (U.S. Pat. No. 6,191,567).

With regard to claims 1, 4, 6-10, 13-15, 18, 20-24, 27-29, 32, 34-38, 41-43, 49-53, 56-58, 64-68, 71-73, 79-83, 86 and 87, Sluijs(i.e., Fig. 2) shows a control system for controlling an output regulator and a method thereof comprising a digital controller (CNTRL), responsive to a sense signal corresponding to a voltage regulated output (Uo) for generating a drive signal to control the power stage, the controller including and selecting between at least three operating modes (i.e., window conversion mode, down-conversion mode, up-conversion mode, see abstract), a selected one of those operating modes to generating a drive signal, the at least three operating modes may include pulse width modulating modes (i.e., duty cycle of the binary (0, 1) signal BS (col. 4, line 63- col. 5, line 5, line 20)), constant on-time modes, constant off-time modes (i.e., "in the window conversion mode each switch (S1-S4) in the converter is

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permanently closed or open (abstract, lines 16-18), voltage modes (i.e., "in the down-conversion mode in order to achieve the conversion from 10V to 3V, and subsequently the desired output voltage was changed to 12V", col. 1, lines 65-67), the digital controller further generating a duty cycle estimation for determining and adjusting the duty cycle of the switch to control the power stage (DMNS, col. 5, lines 5-20), the digital controller having a switching mode selected from a group of synchronous switching (i.e., "each switch (S1-S4) in the converter is permanently closed or open" (abstract, lines 16-18), asynchronous switching (i.e., "in the up-conversion mode the first switch (S) is permanently closed, the second switch (S2) is permanently open" claim 9, col. 8, lines 17-19), and multi-frequency switching (i.e., for different operating modes), the sense signal representing a difference between a reference (RFH, RFL) and the regulated output which is selected to set a nominal value ("desired output voltage of 12V" col. 2, lines 7-8).

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 2, 3, 16-17, 30, 31, 47, 48, 62, 63, 77 and 78 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sluijs in view of Imai et al. (U.S. Pat. No. 6,791,305).

With regard to claims 2, 3, 16-17, 30, 31, 47, 48, 62, 63, 77 and 78, Sluijs shows a control system for controlling an output regulator and a method thereof comprising all the claimed subject matter as discussed above, except for a clock for generating a clock signal.

Imai et al. discloses a switching power supply control circuit which includes a clock for generating clock signals (CLK1, CLK2, CLK3, Fig. 1).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the clock as shown in Imai et al. into the output regulator control system of Sluijs for the purpose of giving the system more precisely results at selected operating modes.

4. Claims 5, 11, 12, 19, 25, 26, 33, 39, 40, 46, 54, 55, 61, 69, 70, 76, 84 and 85 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sluijs in view of Moriguchi et al. (U.S. Pat. No. 6,115,266).

With regard to claims 5, 11, 12, 19, 25, 26, 33, 39, 40, 46, 54, 55, 61, 69, 70, 76, 84 and 85, Sluijs shows a control system for controlling an output regulator and a method thereof comprising all the claimed subject matter as discussed above, except for a current sensor for sensing the output current, and a current reference (note that the control system of Sluijs has an output voltage sensor). Moriguchi et al. (Fig. 3) discloses a power supply controlling circuit that includes a current sensor (24) for sensing the output current, and a reference current (34).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the current sensor and the reference current as shown in Moriguchi et al. into the output regulator control system of Sluijs for the purpose of giving the system a better control and adjust via the help of the output current sensor (beside the output voltage sensor).

5. Claims 44, 59 and 74 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sluijs in view of Kimball et al. (U.S. Pat. No. 6,661,210).

With regard to claims 44, 59 and 74, Sluijs shows a control system for controlling an output regulator and a method thereof comprising all the claimed subject matter as discussed above, except for a linear regulator (note that the control system of Sluijs has a switching regulator).

Kimball et al. (Fig. 3) discloses a power conversion control circuit that includes a linear regulator (42).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the linear regulator as shown in Kimball et al. into the output regulator control system of Sluijs for the purpose of enhancing the power efficiency of the system via the help of the linear regulator (beside the switching regulator).

6. Claims 45, 60 and 75 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sluijs in view of Hua et al. (U.S. Pat. No. 5,486,752).

With regard to claims 45, 60 and 75, Sluijs shows a control system for controlling an output regulator and a method thereof comprising all the claimed subject

matter as discussed above, except for the switching regulator selecting for the group consisting of buck, boost, Cuk, zeta, buck-boost and sepic.

Hua et al. shows a switching power conversion circuit that includes buck (Fig. 6a), boost (Fig. 6b), Cuk (Fig. 6d), zeta (Fig. 6f), buck-boost (Fig. 6c) and sepic (Fig. 6e).

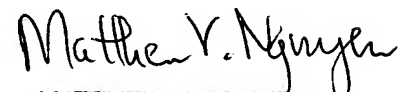
It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the topology of buck, boost, Cuk, zeta, buck-boost and sepic as shown in Hua et al. into the output regulator control system of Sluijs for the purpose of simplifying the system with all kind of basic topologies of the switching regulator.

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Caine et al. (U.S. Pat. No. 6,853,173) also discloses a power conversion system which comprises a digital controller for controlling the power switch in response to a comparison of a sensing output voltage and a reference voltage.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew V. Nguyen whose telephone number is (571) 272-2081.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-2800.

  
MATTHEW V. NGUYEN  
PRIMARY EXAMINER